REMARKS:

In the Office Action, the Examiner rejected claims 1-16 under 35 U.S.C. §112 on the basis that the independent claims recite a single means limitation which covers every conceivable structure for achieving the stated result and therefore is not enabled by the description. The Applicant has therefore amended the claims to replace the term "means for" with structural features of the devices, and to ensure that no "single means" is present.

Independent Claims 1, 8 and 16 now relate to a device, a host and a system comprising a device and a host. The device is for attachment to a host for serial data communication and comprises a predetermined data structure that indicates whether or not the device supports direct memory access. The device also comprises an interface which enables the predetermined data structure to be transferred to the host.

Claims 19-24 are newly added, where newly added independent claim 22 relates to an associated method.

The invention provides a mechanism whereby the host can determine which devices allow direct memory access (DMA). This enables the host to select the device which is most efficient for its purpose. This also allows the host flexibility in scheduling the transfer of data across the bus and allows the host to optimize the use of the device.

In the Office Action, the Examiner has also rejected claims 1-16 under 35 U.S.C. §102(b) on the basis that they are anticipated by Story (US 5,845,151).

Story discloses a desktop PC system having direct memory access (DMA) for transferring data to and from the memory of the desktop PC system. The system comprises a bus controller, a DMA controller, a hardware state machine for programming the DMA controller, and a USB controller.

The system is configured to enable peripheral devices to take over transactions on their own behalf.

The bus controller implements memory data transfer requests from the DMA controller and hardware state machine means. The DMA controller is used for transferring data to and from the memory of the system. The hardware state machine comprises a list of descriptors which describes each data transfer that the hardware state machine initiates controls and completes. Each peripheral device is represented by a separate descriptor. The USB controller is used for receiving and responding to command signals from the hardware state machine and transferring data to and from the DMA controller means and generating and returning a completion status to the hardware state machine after the transfer of data is complete.

Story relates mainly to the host computer and only refers to the peripheral devices briefly. There is no reference in Story to any device which may be attached to the host or a device which comprises a predetermined data structure that indicates whether the device supports DMA as stated by the claims. Therefore Story does not disclose all of the features of the independent claims.

With regards to independent claim 8, although Story discloses that a list of descriptors may be stored in the hardware state machine, there is no indication that any of the descriptors indicate whether or not a device attached to the host supports direct memory access. Furthermore there is no disclosure in Story of such a predetermined data structure being received from a device attached to the host or being identified by the host as a predetermined data structure that indicates whether or not the attached device can support DMA.

There would be no reason why a person skilled in the art would modify the teaching of Story to produce the claimed invention.

There is nothing in Story which discloses or suggests a predetermined data structure which specifically indicates whether a device supports direct memory access. Story does not disclose

that the descriptors stored in the hardware state machine indicate whether an attached device supports DMA, only that the descriptors describe each data transfer that the hardware state machine initiates, controls and completes. The Applicant maintains that it is only with hindsight that the Examiner has equated these descriptors to the predetermined data structures of the present invention which are stored in the devices attached to the host and then transferred to the host.

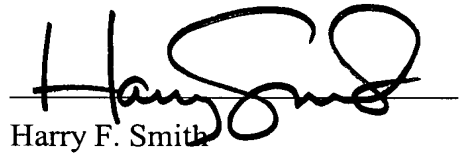
Furthermore, as Story does not explicitly relate to devices which are attached to the host there is no teaching in Story which would suggest modifying a device for attachment to a host to store a predetermined data structure that indicates whether the device supports DMA, as recited in the claims.

Therefore the Applicant maintains that the invention as defined by the amended claims is new and non-obvious with respect to the cited prior art.

In the Office Action, the Examiner has also objected to fig 1 on the basis that he believes it relates to a prior art system and therefore should be labeled as such. However the applicant maintains that this is not the case, as the description clearly describes each feature of the system illustrated in fig 1 in terms of the present invention.

The Examiner is respectfully requested to reconsider and remove the rejections of claims 1-16 under 35 U.S.C. §112 and 35 U.S.C. §102(b) and to allow all of the pending claims as now presented for examination. For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record. Should any unresolved issue remain, the Examiner is invited to call Applicants' agent at the telephone number indicated below.

Respectfully submitted:



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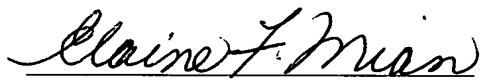

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